DAY 03/30

EMBEDDED SYSTEM DESIGN & IOT

MASTERCLASS

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19+ YEARS OF EXPERIENCE

What you will Learn Today?

- ✓ What is UART
- ✓ Steps for UART TRANSMIT
- ✓ UART DEMO

Announcement

- ✓ Attendance Link at End of the Session
- ✓ Minimum attendance required for an E-Certificate is 28 Days. Attendance link will be valid for 1 hrs. after the event.
- ✓ For Internship Candidates no attendance required ,it will be accessed from the LMS Portal. (learn.pantechsolutions.net)
- ✓ Recorded Video Streaming for LAB classes to improve Learning Experience
- ✓ Videos will be removed from Youtube after 3-5 Days
- ✓ Be Active on facebook group

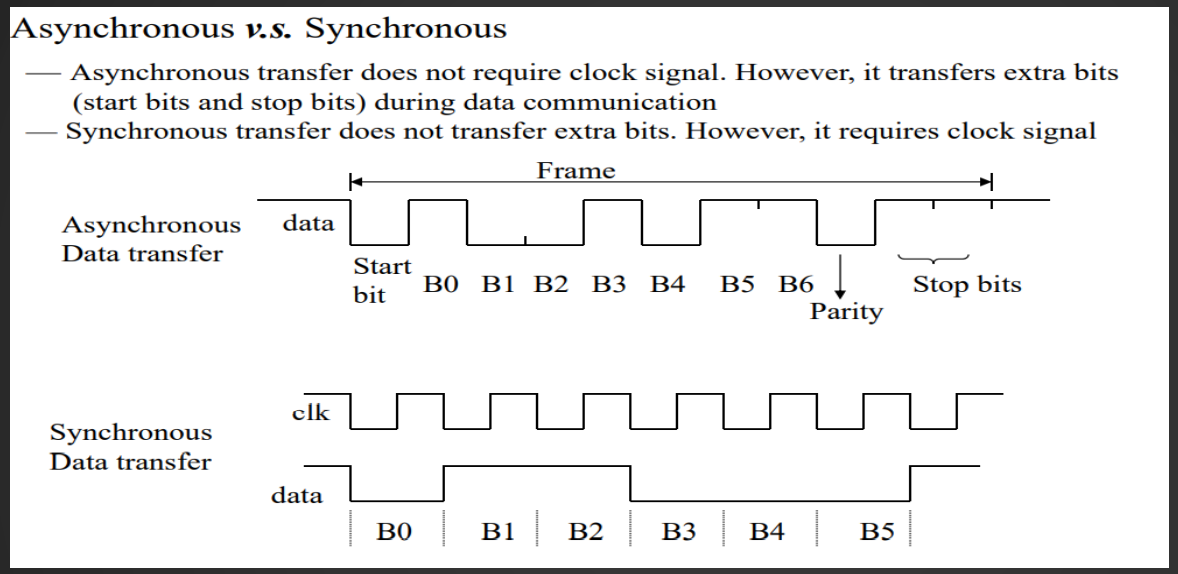
Materials Required

- STM32F411 Nucleo Board

What is a UART?

- **Universal asynchronous receiver and Transmitter**
- **Serial port, COM port, RS232, RS485**
- **VERY COMMON AND SIMPLE**
- **Useful for communication to**
  - Microcontroller
  - Computer
  - Other FPGA

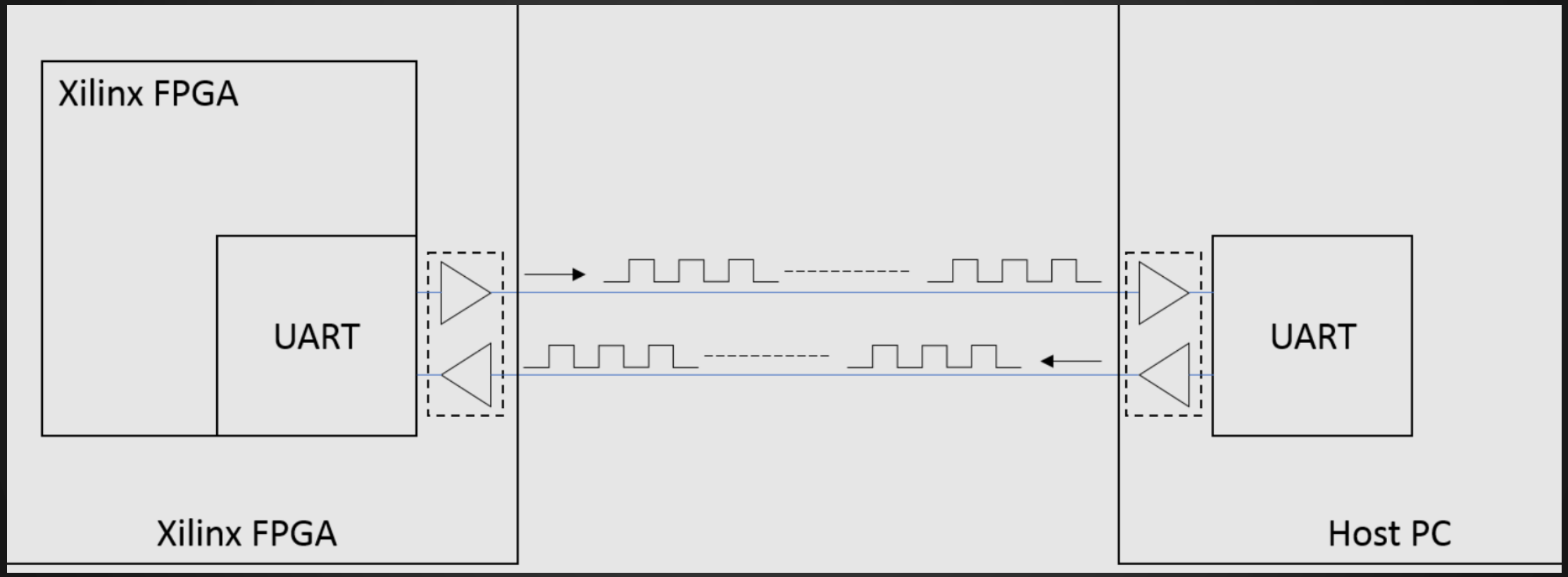
Asynchronous Vs Synchronous



Two methods of serial communication are

- Synchronous Communication: Transfer of bulk data in the framed structure at a time
- Asynchronous Communication: Transfer of a byte data in the framed structure at a time

UART



UART Parameters

- Baud Rate (9600, 19200, 115200, others)
- Number of Data Bits (7, 8)
- Parity Bit (On, Off)
- Stop Bits (0, 1, 2)
- Flow Control (None, On, Hardware)

STEPS FOR UART TRANSMIT

//Enable clocK access to GPIOA

//SET PA2 MOODE TO Alternate function Mode

//SET PA2 Alternative function type to UART_TX (AF07)

//CONFIGURE UART MODULE

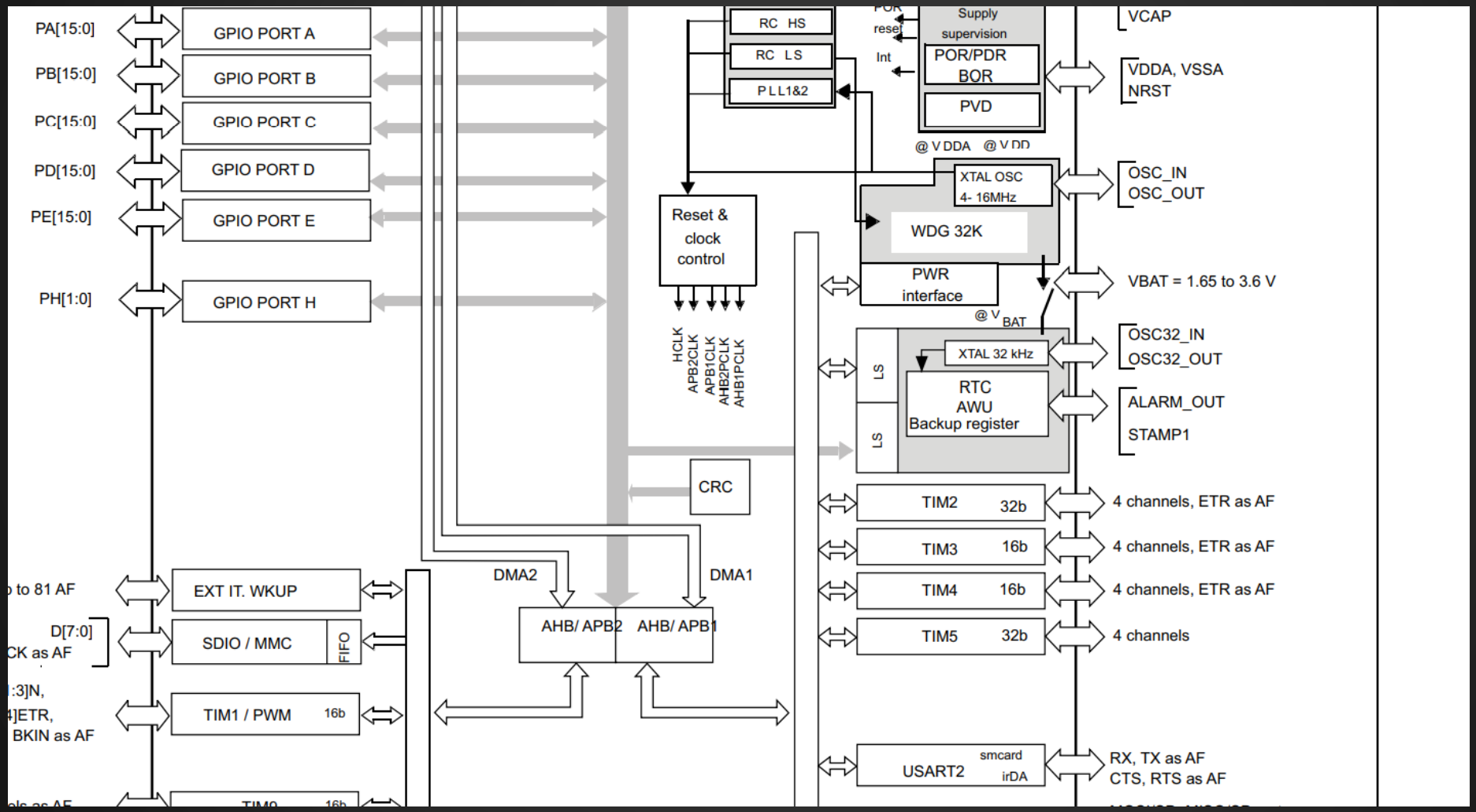
//ENABLE CLOCK ACCESS TO UART2

//CONFIGURE BAUDRATE

//CONFIGURE TRANSFER DIRECTION

//ENABLE UART MODULE

Block Diagram



Associated GPIO

UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100	Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
10	14	F6	23	L2	PA0-WKUP	I/O	TC	(5)	TIM2_CH1/TIM2_ET, TIM5_CH1, USART2_CTS, EVENTOUT	ADC1_0, WKUP1
11	15	G7	24	M2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, EVENTOUT	ADC1_1
12	16	E5	25	K3	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, EVENTOUT	ADC1_2
13	17	E4	26	L3	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, EVENTOUT	ADC1_3

FUNCTIONAL MAPPING

Table 9. Alternate function mapping

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/I2S1SPI2/ I2S2/SPI3/ I2S3	SPI2/I2S2/ SPI3/ I2S3/SPI4/ I2S4/SPI5/ I2S5	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	-	-	-	-	USART2_ CTS	-	-	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI /I2S4_SD	-	USART2_ RTS	-	-	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_ TX	-	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_ RX	-	-	-	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS/I 2S1_WS	SPI3_NSS/I2 S3_WS	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_SCK/I 2S1_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	-	-	SPI1_MISO	I2S2_MCK	-	-	-	-	-	SDIO_ CMD	-	-	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	-	-	SPI1_MOSI /I2S1_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	USB_FS_ SOF	-	SDIO_ D1	-	-	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_ TX	-	-	USB_FS_ VBUS	-	SDIO_ D2	-	-	EVENT OUT

ALTERNATE FUNCTIONS

Address offset: 0x20
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFRL7[3:0]				AFRL6[3:0]				AFRL5[3:0]				AFRL4[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFRL3[3:0]				AFRL2[3:0]				AFRL1[3:0]				AFRL0[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
				0	1	1	1								

Bits 31:0 **AFRLy:** Alternate function selection for port x bit y (y = 0..7)
These bits are written by software to configure alternate function I/Os

AFRLy selection:

0000: AF0	1000: AF8
0001: AF1	1001: AF9
0010: AF2	1010: AF10
0011: AF3	1011: AF11
0100: AF4	1100: AF12
0101: AF5	1101: AF13
0110: AF6	1110: AF14
0111: AF7	1111: AF15

BAUD RATE CALCULATION

- Peripheral Clock =16000000
- BAUDRATE=9600
- BRR =((16000000+(9600/2))/9600)
- BRR= 1667
- HEX VALUE OF BRR =0X0683

UART WRITE

```
7  void uart2_write(int ch)
8  {
9      //Make sure the transmit data register is empty
0      while(!(*USART2_SR & 0x0080)){}
1      //write to transmit data register
2      *USART2_DR =(ch&0XFF);
3  }
```

TXE: Transmit data register empty

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TXEIE bit =1 in the USART_CR1 register. It is cleared by a write to the USART_DR register.

0: Data is not transferred to the shift register

1: Data is transferred to the shift register)

26.6.1 Status register (USART_SR)

Address offset: 0x00

Reset value: 0x00C0 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
						rc_w0	rc_w0	r	rc_w0	rc_w0	r	r	r	r	r

USART DATA REGISTER

Data register (USART_DR)

Address offset: 0x04

Reset value: 0xXXXX XXXX

Bits 31:9 Reserved, must be kept at reset value

Bits 8:0 **DR[8:0]**: Data value

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR)

The TDR register provides the parallel interface between the internal bus and the output shift register (see Figure 1).

The RDR register provides the parallel interface between the input shift register and the internal bus.

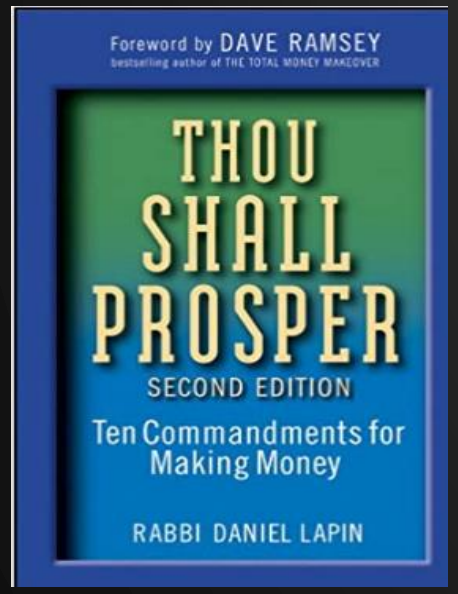
When transmitting with the parity enabled (PCE bit set to 1 in the USART_CR1 register), the value written in the MSB (bit 7 or bit 8 depending on the data length) has no effect because it is replaced by the parity.

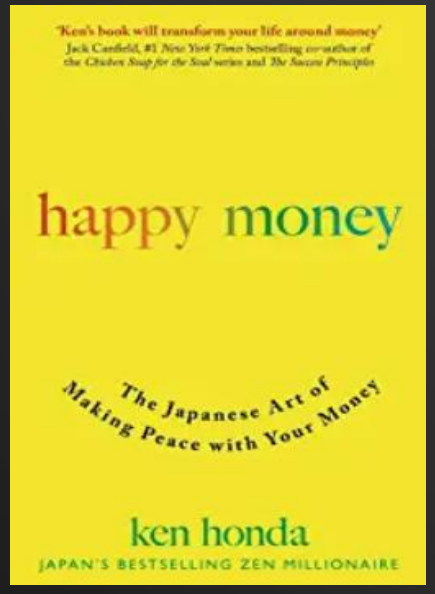
When receiving with the parity enabled, the value read in the MSB bit is the received parity bit.

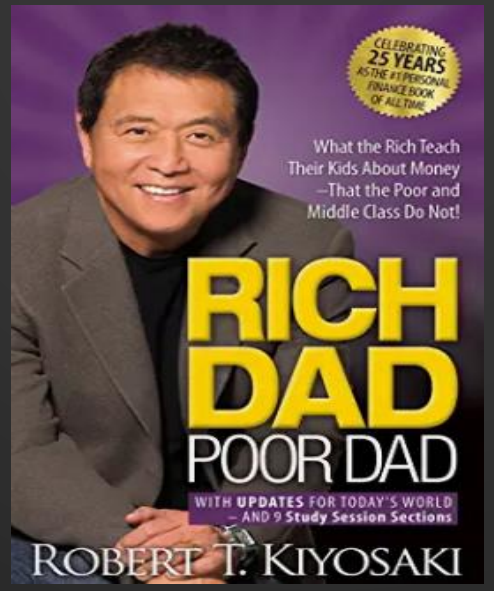
DEMO

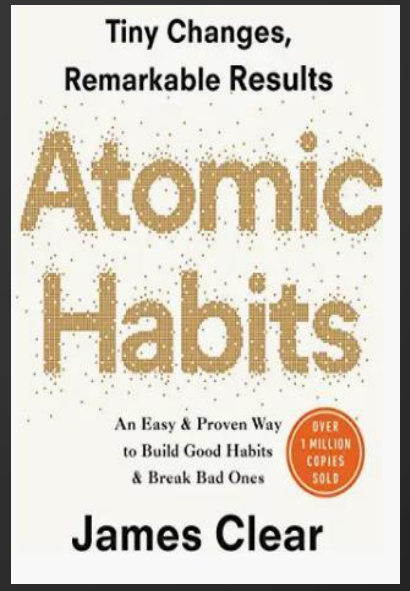
Mindset Lesson

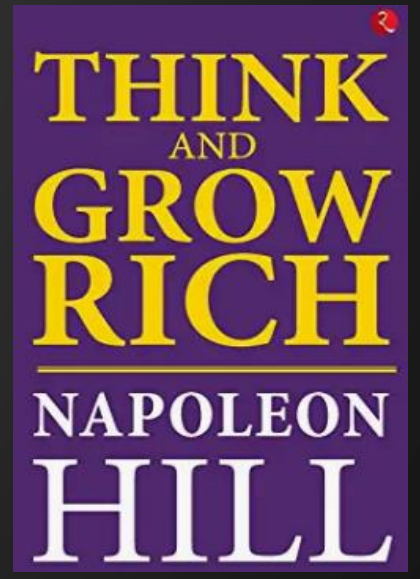
- ✓ Managing Money is more important than making Money
- ✓ Money Mindset – Scarcity /Abundance











Mindset Activity

- ✓ Write Down Your Top 10 Goals.(1 Mark)
- ✓ Write Down Your Top 10 Ideas to Achieve Your Goal.(1 Mark)
- ✓ 30 Minutes for Workout (5000-7000 Steps a Day)(2 Mark).
- ✓ 15 Minutes to Meditate (2 Mark)
- ✓ 10 Minutes to Visualize of Achieving Your Goals(1)
- ✓ 10 Minutes to Focus on the Day Plan (1)
- ✓ 2 Hr's for Learning and Take Notes. (2 Mark)

10/10

https://www.facebook.com/groups/embeddedsystemsandiot/

THANK YOU